

Fig. 1A PRIOR ART

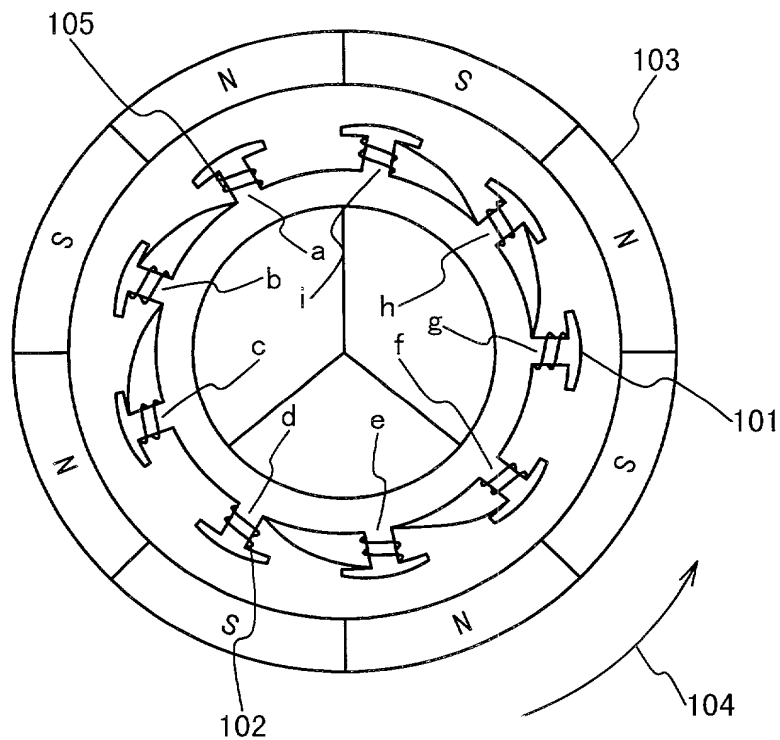


Fig. 1B PRIOR ART

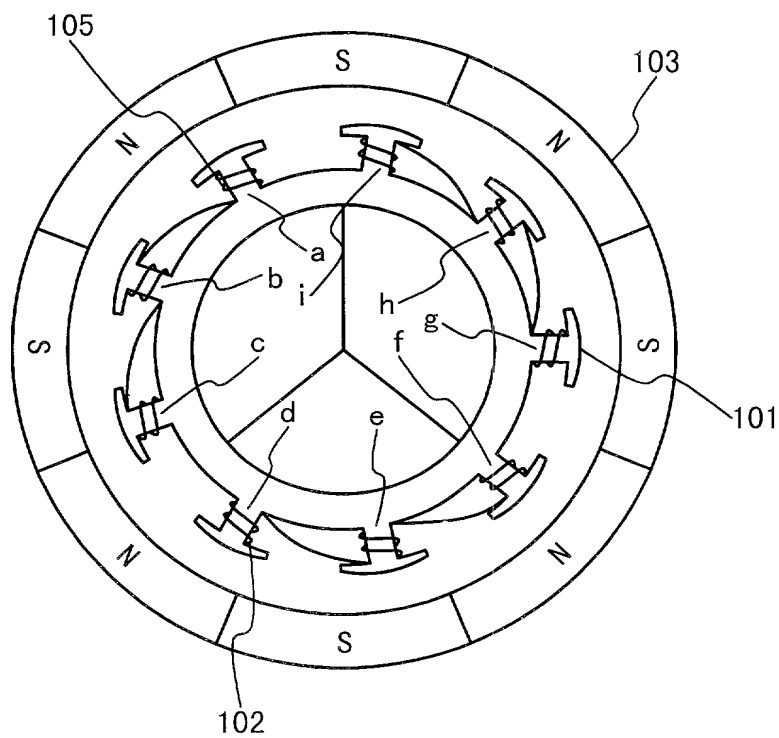


Fig. 2 PRIOR ART

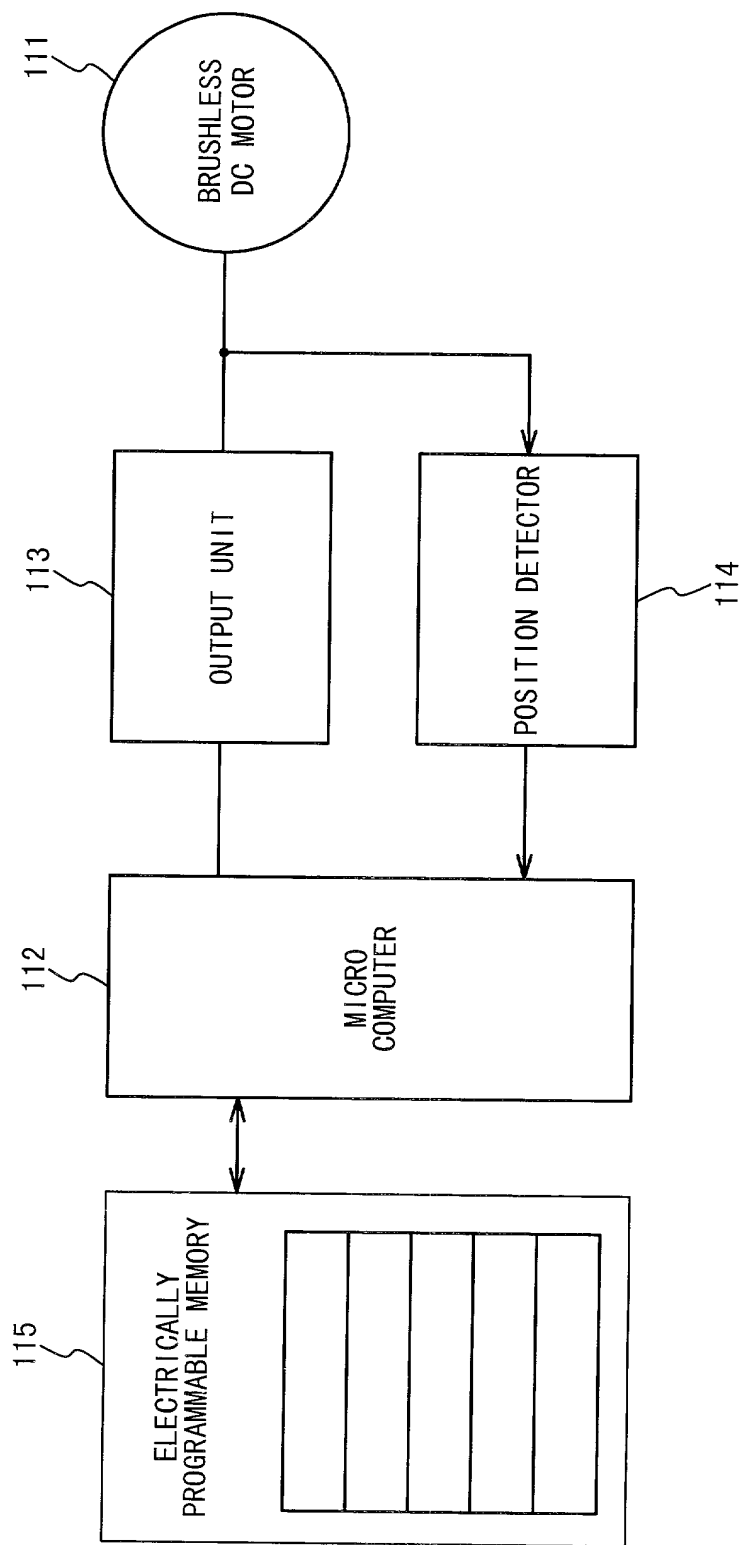


Fig. 3A PRIOR ART

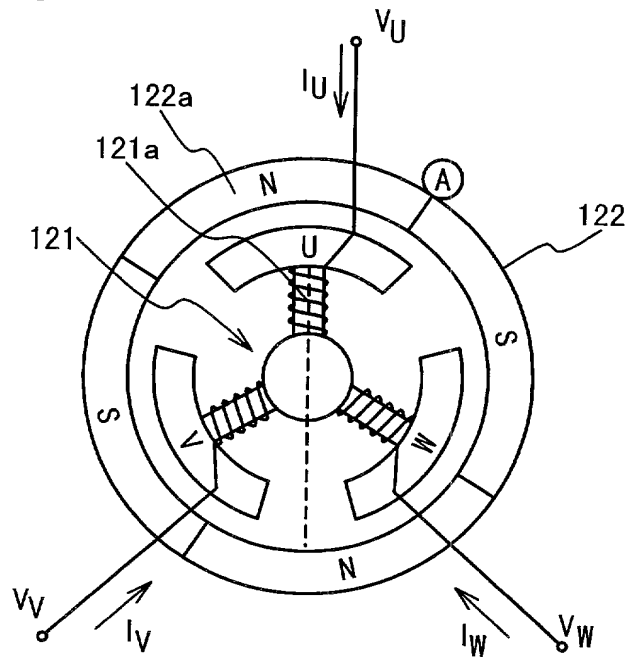


Fig. 3B PRIOR ART

TIMING	(1)	(2)	(3)	(4)	(5)	(6)
U PHASE DRIVE VOLTAGE $V_U$	$V_{CC}$	$V_{CC}$	N. C.	GND	GND	N. C.
V PHASE DRIVE VOLTAGE $V_V$	GND	N. C.	$V_{CC}$	$V_{CC}$	N. C.	GND
W PHASE DRIVE VOLTAGE $V_W$	N. C.	GND	GND	N. C.	$V_{CC}$	$V_{CC}$

Fig. 3C PRIOR ART

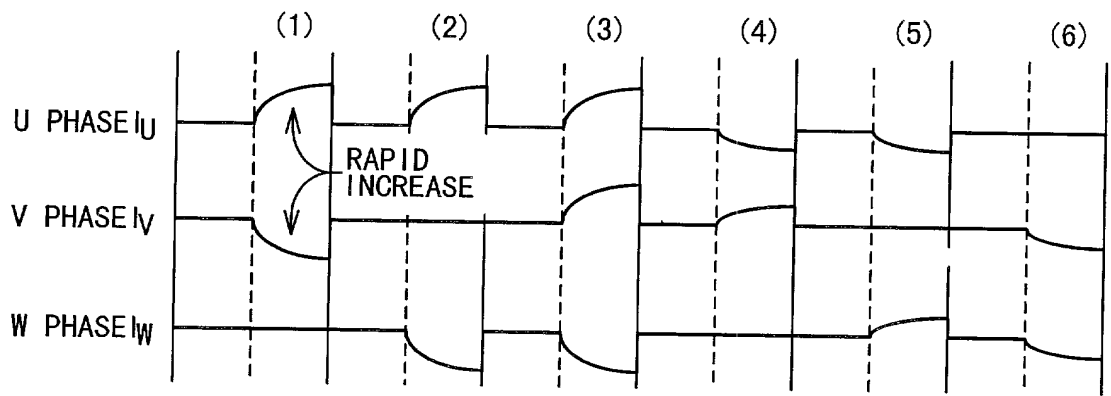


Fig. 4

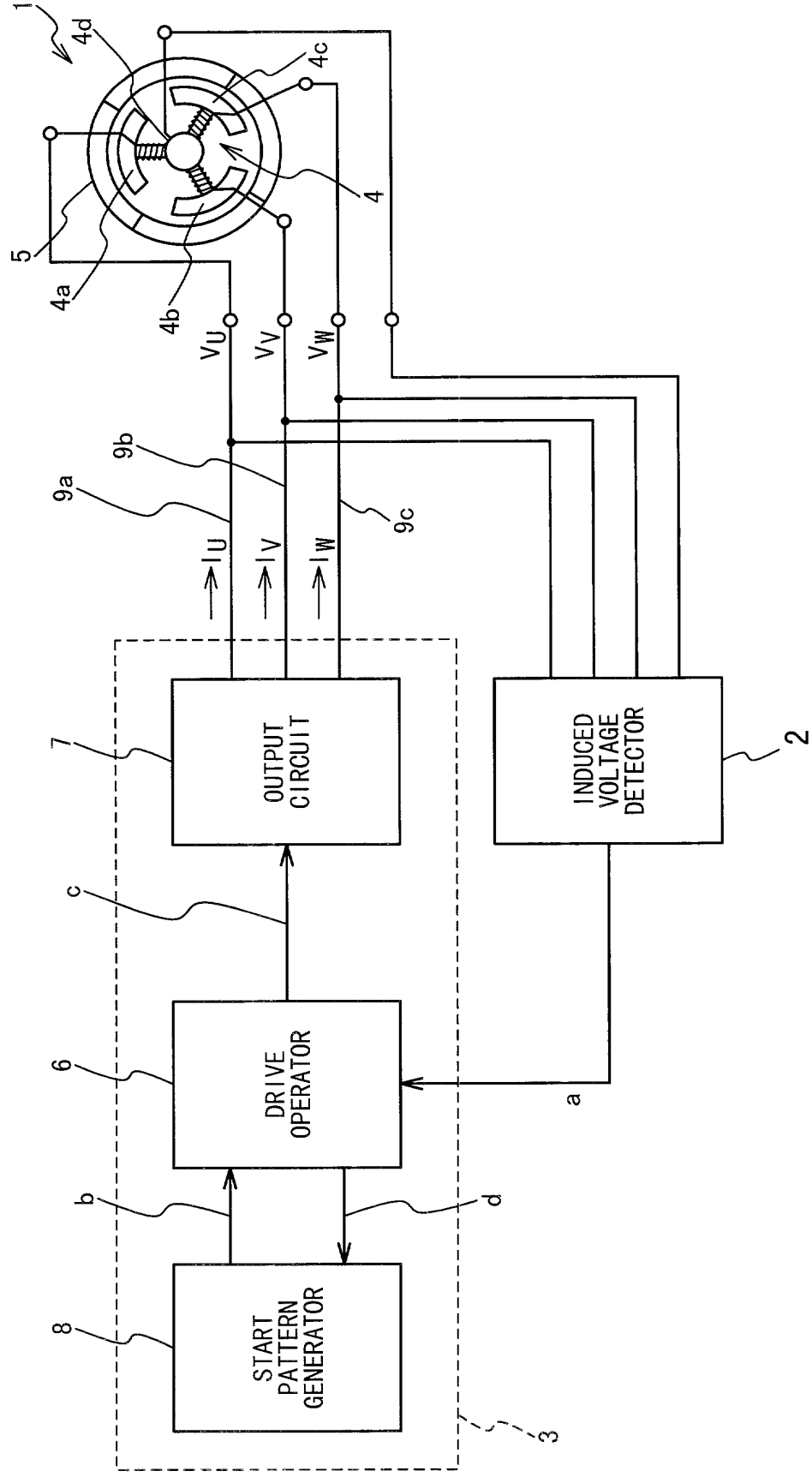
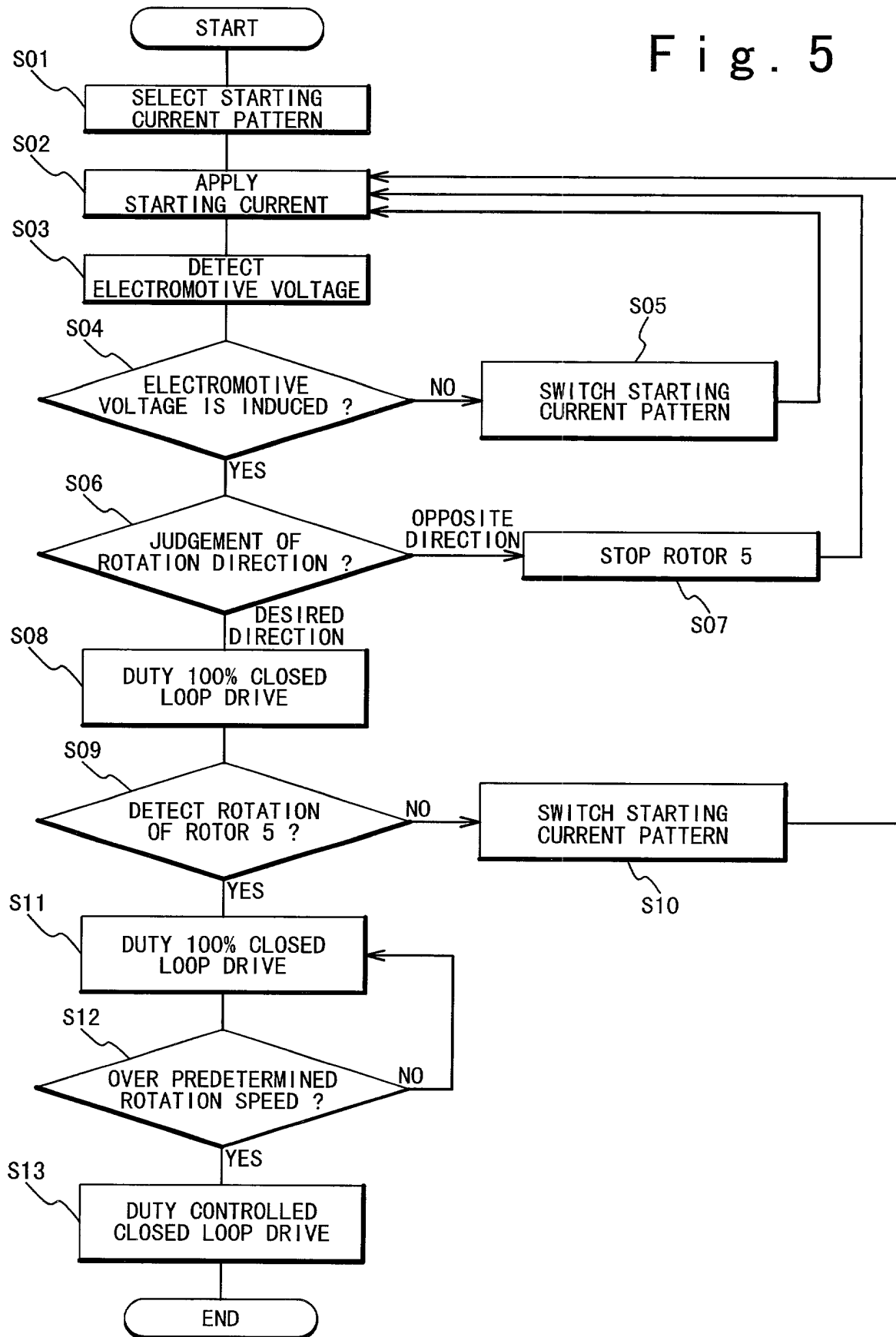


Fig. 5



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STRTING CURRENT PATTERN	STARTING CURRENT	U PHASE LINE 9a	V PHASE LINE 9b	V PHASE LINE 9c
PATTERN 1	V→U	GND	V <sub>CC</sub>	NC
PATTERN 2	V→W	NC	V <sub>CC</sub>	GND
PATTERN 3	U→W	V <sub>CC</sub>	NC	GND
PATTERN 4	U→V	V <sub>CC</sub>	GND	NC
PATTERN 5	W→V	NC	GND	V <sub>CC</sub>
PATTERN 6	W→U	GND	NC	V <sub>CC</sub>

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